AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor processing device ~~being~~ capable of inputting/outputting encrypted data from/to an outside of the device and ~~being~~ formed over a semiconductor substrate, the device comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit; and

a central processing unit,

wherein the first non-volatile memory is used for storing an encryption key to be used for encrypting the data, and the second non-volatile memory is used for storing a program to be processed by the central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory ~~has~~includes a plurality of non-volatile memory cells,

wherein each of the non-volatile memory cells ~~has~~includes

a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate,

~~has~~ an electric charge storage layer ~~on~~ over the channel region ~~through a first insulating film~~,

~~has~~ a first gate terminal ~~on~~ over the electric charge storage layer ~~through a second insulating film~~,

~~and has~~ a second gate terminal ~~through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer~~ over the channel region,

a first insulating film on the channel region under the electric charge storage layer and the second gate terminal, and

a second insulating film between the electric charge storage layer and the first gate terminal,

wherein the semiconductor processing device is constructed to carry out an operation for changing a threshold voltage of the memory cell by injecting a hot electron generated in the channel region provided under ~~the~~ a third insulating film ~~is injected~~ into the electric charge storage layer or by extracting an electric charge ~~is extracted~~ from the electric charge storage layer, ~~thereby~~

~~carrying out an operation for changing a threshold voltage of the memory cell~~

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes

the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

2. (original) The semiconductor processing device according to claim 1,

wherein the first non-volatile memory is further used for storing information to be utilized for specifying an individual.

3. (currently amended) The semiconductor processing device according to claim 2,

wherein ~~the~~ a first data length is smaller than ~~the~~ a second data length.

4. (currently amended) The semiconductor processing device according to claim 3, further comprising:

a terminal ~~to be used~~ for ~~an~~ input/output from/to an outside of the semiconductor processing device,

the program being supplied from the outside through the terminal and stored in the second non-volatile memory.

5. (currently amended) The semiconductor processing device according to claim 4,

wherein the central processing unit ~~can give~~ accesses ~~to~~ the first non-volatile memory and the second non-volatile memory in parallel.

6. (currently amended) The semiconductor processing device according to claim 5,

wherein the first non-volatile memory has a memory array portion ~~constituted by~~ comprising a plurality of memory cells and a control portion for controlling access to a selected memory cell,

wherein the second non-volatile memory has a memory array portion ~~constituted by~~ comprising a plurality of memory cells and a control portion for controlling access to a selected memory cell, and

wherein the control portion of the first non-volatile memory and the control portion of the second non-volatile memory are ~~common~~ at least partially common.

7. (currently amended) The semiconductor processing device according to claim 6,

wherein a common part of the control portion ~~to be common~~ is an amplifier circuit ~~to be used~~ for amplifying a read signal when data are ~~to be~~ read from a memory cell.

8. (currently amended) The semiconductor processing device according to claim 6,

wherein a common part of the control portion ~~to be common~~ is a voltage generating circuit for generating a voltage ~~to be~~ applied to a memory cell when access is ~~to be~~ given to the memory cell.

9. (currently amended) The semiconductor processing device according to claim 6,

wherein a common part of the control portion ~~to be common~~ is a decoder circuit for selecting a memory cell when access is ~~to be~~ given to the memory cell.

10. (currently amended) An IC card ~~being~~ enclosed with a synthetic resin, comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

a terminal for inputting/outputting data from/to an outside of the IC card,

wherein encrypted data are input/output from/to the outside of the IC card,

wherein the first non-volatile memory is used for storing an encryption key to be utilized for encrypting the data, and the second non-volatile memory is used for storing a program to be processed by the central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory ~~has~~includes a plurality of non-volatile memory cells,

wherein each of the non-volatile memory cells ~~has~~ includes

a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate,

~~has~~ an electric charge storage layer ~~on~~ over the channel region ~~through a first insulating film~~,

~~has~~ a first gate terminal ~~on~~ over the electric charge storage layer ~~through a second insulating film~~,

~~and has~~ a second gate terminal ~~through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer~~ over the channel region,

a first insulating film on the channel region under the electric charge storage layer and the second gate terminal, and

a second insulating film between the electric charge storage layer and the first gate terminal,

wherein the semiconductor processing device is constructed to carry out an operation for changing a threshold voltage of the memory cell by injecting a hot electron generated in the channel region provided under ~~the~~ a third insulating film ~~is injected~~ into the electric charge storage layer or by extracting an electric charge ~~is extracted~~ from the electric charge storage layer, ~~thereby carrying out an operation for changing a threshold voltage of the memory cell~~,

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

11. (currently amended) An IC card ~~being~~ enclosed with a synthetic resin, comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

an antenna for inputting/outputting data from/to an outside of the IC card,

wherein encrypted data are input/output from/to the outside of the IC card,

wherein the first non-volatile memory is used for storing an encryption key to be utilized for encrypting the data, and the second non-volatile memory is used for storing a program to be processed by the central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory ~~has~~includes a plurality of non-volatile memory cells,

wherein each of the non-volatile memory cells ~~has~~ includes

a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate,

~~has~~ an electric charge storage layer ~~on~~ over the channel region ~~through a first insulating film~~,

~~has~~ a first gate terminal ~~on~~ over the electric charge storage layer ~~through a second insulating film~~,

~~and has~~ a second gate terminal ~~through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer~~ over the channel region,

a first insulating film on the channel region under the electric charge storage layer and the second gate terminal, and

a second insulating film between the electric charge storage layer and the first gate terminal,

wherein the semiconductor processing device is constructed to carry out an operation for changing a threshold voltage of the memory cell by injecting a hot electron generated in the channel region provided under ~~the~~ a third insulating film ~~is injected~~ into the electric charge storage layer or by extracting an electric charge ~~is extracted~~ from the electric charge storage layer, ~~thereby carrying out an operation for changing a threshold voltage of the memory cell~~,

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

Claims 12-13. (cancelled)

14. (currently amended) A semiconductor processing device ~~being~~ capable of inputting/outputting encrypted data to/from an outside of the device, the device comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit; and

a central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory has a plurality of memory cells,

wherein each of the memory cells ~~has~~ includes

a source region,

a drain region and

a channel region between the source region and the drain region,

~~has~~ a data storage insulating layer and a first gate ~~on~~ over the channel region ~~through an insulating layer~~, and

~~has~~ a second gate ~~on~~ over the data storage insulating layer,

wherein each of the first non-volatile memory and the second non-volatile memory ~~has~~ includes a plurality of first word lines, in which corresponding memory cells are connected to the first word lines when the stored information is erased from the first non-volatile memory, corresponding memory cells are connected to the first word lines when the stored information is erased from the second non-volatile memory, and ~~the~~ a number of the memory cells to be connected to the first word lines in the first non-volatile memory is smaller than ~~that~~ a number of the memory cells to be connected to the first word lines in the second non-volatile memory,

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes

the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

Claims 15-16. (cancelled)

17. (currently amended) The semiconductor processing device according to claim [[16]]14,

wherein the switch ~~unit~~ circuit is ~~an~~ a MOS transistor of ~~the~~ a same conductive type as the non-volatile memory cell.

18. (currently amended) A semiconductor processing device comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

an external interface circuit,

wherein the first non-volatile memory is used for storing data, and the second non-volatile memory is used for storing a program to be processed by the central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

wherein each of the non-volatile memory cells ~~has~~ includes

a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate,

~~has~~ an electric charge storage layer ~~on~~ over the channel region ~~through a first insulating film~~,

~~has~~ a first gate terminal ~~on~~ over the electric charge storage layer ~~through a second insulating film~~, ~~and~~

~~has~~ a second gate terminal ~~through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer~~ over the channel region,

a second insulating film between the electric charge storage layer and the first gate terminal, and

a third insulating film between the channel region and the second gate terminal,

wherein the semiconductor processing device is constructed to carry out an operation for changing a threshold voltage of the memory cell by injecting a hot electron generated in the channel region provided under ~~the~~ a third insulating film ~~is injected~~ into the electric charge storage layer or by extracting an electric charge ~~is extracted~~ from the electric charge storage layer, ~~thereby~~

~~carrying out an operation for changing a threshold voltage of the memory cell~~,

wherein ~~the~~ a first data length is smaller than ~~the~~ a second data length,

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes

the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

19. (currently amended) The semiconductor processing device according to claim 18,

wherein ~~the non-volatile memory cell has a source region, a drain region, and a channel region interposed between the source region and the drain region on a semiconductor substrate, a control gate electrode provided through a first insulating film and a memory gate electrode provided through a second insulating film and an electric charge storage insulating film and isolated electrically from the control gate electrode are provided on the channel region, and~~ a gate breakdown voltage of the ~~control gate electrode~~second gate terminal is lower than that of the ~~memory gate electrode~~first gate terminal.

20. (currently amended) The semiconductor processing device according to claim 19,

wherein the gate breakdown voltage of the ~~control gate electrode~~second gate terminal is equal to that of ~~an~~ a MOS transistor included in the ~~CPU~~central processing unit.

Claims 21-22. (cancelled)

23. (currently amended) The semiconductor processing device according to claim 19,

wherein the central processing unit ~~can give access to~~accesses the first non-volatile memory and the second non-volatile memory in parallel.

24. (currently amended) The semiconductor processing device according to claim 23,

wherein the first non-volatile memory has a memory array portion ~~constituted by~~comprising a plurality of memory cells and a control portion for controlling access to a selected memory cell,

wherein the second non-volatile memory has a memory array portion ~~constituted by~~comprising a plurality of memory cells and a control portion for controlling access to a selected memory cell, and

wherein the control portion of the first non-volatile memory and the control portion of the second non-volatile memory are ~~common~~ at least partially common.

25. (currently amended) The semiconductor processing device according to claim 24,

wherein a common part of the control portion ~~to be common~~ is an amplifier circuit ~~to be used~~ for amplifying a read signal when data are ~~to be~~ read from a memory cell.

26. (currently amended) The semiconductor processing device according to claim 24,

wherein a common part of the control portion ~~to be common~~ is a voltage generating circuit for generating a voltage to be applied to a memory cell when access is ~~to be~~ given to the memory cell.

27. (currently amended0 The semiconductor processing device according to claim 24,

wherein a common part of the control portion ~~to be common~~ is a decoder circuit for selecting a memory cell when access is ~~to be~~ given to the memory cell.

28. (currently amended) An IC card ~~being~~ enclosed with a synthetic resin, comprising:

a first non-volatile memory for erasing stored information on a first data length unit;

a second non-volatile memory for erasing stored information on a second data length unit;

a central processing unit; and

a terminal for inputting/outputting data from/to an outside of the IC card,

wherein the first non-volatile memory is used for storing data, and the second non-volatile memory is used for storing a program to be processed by the central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells,

wherein each of the non-volatile memory cells ~~has~~ includes

a first channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate,

~~has~~ an electric charge storage layer on the first channel region ~~through a first insulating film~~,

~~has~~ a first gate terminal on the electric charge storage layer ~~through a second insulating film~~, ~~and~~

~~has~~ a second gate terminal ~~through the first gate terminal and a third insulating film~~ on a second channel region which is adjacent to ~~a~~ the first channel

region provided under the electric charge storage layer,

a first insulating film between the first channel region and the electric charge storage layer,

a second insulating film between the electric charge storage layer and the first gate terminal, and

a third insulating film between the second channel region and the second gate terminal,

wherein the semiconductor processing device is constructed to carry out an operation for changing a threshold voltage of the memory cell by injecting a hot electron generated in the channel region provided under ~~the~~ a third insulating film ~~is injected~~ into the electric charge storage layer or by extracting an electric charge ~~is extracted~~ from the electric charge storage layer, ~~thereby carrying out an operation for changing a threshold voltage of the memory cell~~,

wherein ~~the~~ a first data length is smaller than ~~the~~ a second data length,

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes

the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

29. (currently amended) An IC card comprising:

a first non-volatile memory for erasing stored information on a first data length unit[,];

a second non-volatile memory for erasing stored information on a second data length unit[[,]];

a central processing unit[[,]]; and

an antenna for inputting/outputting data from/to an outside of the IC card;

~~which~~wherein the first non-volatile memory, second non-volatile memory, central processing unit, and antenna are enclosed with a synthetic resin,

wherein the first non-volatile memory is used for storing data, and the second non-volatile memory is used for storing a program to be processed by the central processing unit,

wherein each of the first non-volatile memory and the second non-volatile memory ~~has~~ includes a plurality of non-volatile memory cells,

wherein each of the non-volatile memory cells ~~has~~ includes

a first channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate,

~~has~~ an electric charge storage layer on the channel region ~~through a first insulating film~~,

~~has~~ a first gate terminal on the electric charge storage layer ~~through a second insulating film~~, ~~and~~

~~has~~ a second gate terminal ~~through the first gate terminal and a third insulating film~~ on a second channel region which is adjacent to ~~a~~ the first channel region provided under the electric charge storage layer,

wherein the semiconductor processing device is constructed to carry out an operation for changing a threshold voltage of the memory cell by injecting a hot electron generated in the channel region provided under ~~the~~ a third insulating film ~~is injected~~ into the electric charge storage layer or by extracting an electric charge ~~is extracted~~ from the electric charge storage layer, ~~thereby carrying out an operation for changing a threshold voltage of the memory cell~~,

wherein ~~the~~ a first data length is smaller than ~~the~~ a second data length,

wherein the first non-volatile memory includes

a plurality of switch circuits;

a first control signal line;

a plurality of first control signal sub-lines; and

a second control signal line;

wherein the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit

constructed to select among various ones of said first control signal sub-lines,

wherein the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

wherein the second non-volatile memory includes

the first control signal line and the second control signal line,

wherein the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and

wherein the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

30. (currently amended) The semiconductor processing device according to claim ~~28 or~~ 29,

wherein ~~the non-volatile memory cell has a source region, a drain region, and a channel region interposed between the source region and the drain region on a semiconductor substrate, a control gate electrode provided~~

~~through a first insulating film and a memory gate electrode provided through a second insulating film and an electric charge storage insulating film and isolated electrically from the control gate electrode are provided on the channel region, and~~ a gate breakdown voltage of the ~~control gate electrodes~~second gate terminal is lower than that of the ~~memory gate electrode~~first gate terminal.

31. (currently amended) The semiconductor processing device according to claim 30,

wherein the gate breakdown voltage of the ~~control gate electrode~~ second gate terminal is equal to that of ~~an~~ a MOS transistor included in the ~~CPU~~central processing unit.